Semiconductor memory device and

Semiconductor integrated circuit

Background of the Invention

The present invention relates to a semiconductor

memory device, and to a technology effective if applied

to a semiconductor memory in which static memory cells

are arranged.

In a semiconductor memory device used as one

example of a semiconductor integrated circuit, a latch

circuit for storing and retaining data comprises n

channel type MOS transistors and their load elements. A

signal input/output terminal of the latch circuit and its

corresponding bit line are connected via one of access

transistors. The access transistor is normally configured

as an n channel type MOS transistor. However, when the n

channel type MOS transistor is used in the access

transistor, a cell current at a read operation becomes

small according to the threshold voltage of the n channel

type MOS transistor, its operating speed becomes slow and

the speed of writing of data on the high level side

becomes slow. Therefore, there has been proposed a

semiconductor memory device wherein access transistors

are configured as p channel MOS transistors (e.g., Patent

Documents 1 and 2). In a circuit provided with p channel

MOS transistors as access transistors, the potential of a

storage node, which is stepped or pulled down by the

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corresponding access transistor, extend to a potential higher than a ground potential (power supply VSS on the low potential side) by the threshold voltage of the access transistor. When this potential is higher than a reverse threshold voltage of a latch circuit, the writing of data (or its rewriting) cannot be performed. Therefore, there is known a technology wherein a terminal different from a terminal for supply of a normal power supply potential GND on the low potential side is provided, and the potential higher by a predetermined level than a select level of a word line is supplied to the terminal to thereby make it possible to detect low level data of each bit line by means of a latch circuit even if the potential of a storage node is reduced by a threshold voltage of an access transistor upon a write operation, whereby the writing and rewriting of data can be reliably performed.

[Patent Document 1]

Japanese Unexamined Patent Publication No. Hei 9(1997)-231765

[Patent Document 2]

Japanese Unexamined Patent Publication No. Hei 4(1992)-168694

Summary of the Invention

When a p channel type MOS transistor is used in each access transistor of a memory cell, a node potential

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remains upon writing of a logical value "0" so that a write operation becomes instable. With this view, the supply of a voltage higher by a predetermined level than the normal power supply potential on the low potential side is effective as in the technology described in the Patent Document 1. According to the Patent Document 1, however, a cell area becomes relatively large because the access transistor is formed in a bulk layer. As in a memory cell 1 shown in Fig. 1 of the Patent Document 1, for example, load resistors R11 and R12 can be omitted from a memory cell formed of four transistors Q11 through Q14 and the two load resistors R11 and R12. In such a circuit configuration, however, a cell read current and a leak current are proportional to each other though the area of the memory cell becomes small, so a high speed operation and a low leak of a memory become incompatible. That is, when the threshold voltage is lowered and a sufficient gate-to-source voltage Vgs is ensured for the purpose of the high speed operation, a large standby current flows. When the threshold voltage is made high and a drain-to-source voltage Vds is lowered in reverse, a small read current flows and hence a low speed operation is provided.

An object of the present invention is to provide a technology for achieving a reduction in cell area and the appropriateness of writing of a logical value "0". Another object of the present invention is to provide a

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technology for achieving a reduction in standby current and an increase in operating speed.

The above, other objects and novel features of the present invention become apparent from the description of the present Specification and the accompanying drawings.

Summaries of representative ones of the inventions disclosed in the present application will be described in brief as follows:

There is provided a semiconductor memory device including a first bit line for transferring data; a second bit line having a relationship of complementary levels with the first bit line; a storage section in which a drain electrode of a first transistor and a gate electrode of a second transistor are connected to each other to form a first node, and a drain electrode of the second transistor and a gate electrode of the first transistor are connected to each other to form a second node; a p channel type third transistor capable of connecting the first node to the first bit line in accordance with a voltage level of a word line; a p channel type fourth transistor capable of connecting the second node to the second bit line in accordance with the voltage level of the word line; and a power supply circuit capable of supplying a voltage set on the condition that a difference between a source potential applied to each of the first and second transistors and a potential of a select level of the word line becomes

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greater than or equal to a threshold voltage of each of the third and fourth transistors, to a source electrode of each of the first and second transistors, wherein the third and fourth transistors are configured as a vertical structure, the third transistor is laminated over the first transistor, and the fourth transistor is laminated over the second transistor.

According to the above means, the third and fourth transistors are configured as a vertical structure, the third transistor is laminated over the first transistor, and the fourth transistor is laminated over the second transistor. This achieves a reduction in cell area. The power supply circuit supplies the voltage set on the condition that the difference between the source potential applied to each of the first and second transistors and the potential of the select level of the word line becomes greater than or equal to the threshold voltage of each of the third and fourth transistors, to the source electrode of each of the first and second transistors. Owing to it, "0" write compensation is carried out. This achieves the appropriateness of writing of a logical value "0".

At this time, the potential of the select level of the word line can be set as a ground level. Further, the power supply circuit includes a fifth transistor connected to the source electrodes of the first and second transistors and ground, and an error amplifier for

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determining a difference between a reference voltage supplied thereto and the source potential applied to each of the first and second transistors and controlling on resistance of the fifth transistor, based on the difference.

When a semiconductor memory device is configured which comprises including a first memory cell area in which first memory cells are disposed in an array form, a second memory cell area in which second memory cells different in structure from the first memory cells are disposed in an array form, and a peripheral circuit shared between the first memory cell area and the second memory cell area, each of the first memory cells comprises including a storage section comprising an n channel type first MOS transistor and an n channel type second MOS transistor connected to each other, a p channel type third MOS transistor capable of connecting a drain electrode of the first MOS transistor and a gate electrode of the second MOS transistor to a first bit line, and a p channel type fourth MOS transistor capable of connecting a drain electrode of the second MOS transistor and a gate electrode of the first MOS transistor to the first bit line. The third and fourth MOS transistors can be configured as a vertical structure, the third MOS transistor can be laminated over the first MOS transistor, and the fourth MOS transistor can be laminated over the second MOS transistor. At this time,

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each of the second memory cells includes a storage section in which a first inverter comprising a p channel type fifth MOS transistor and an n channel type sixth MOS transistor both connected in series, and a second inverter comprising a p channel type seventh MOS transistor and an n channel type eighth MOS transistor both connected in series are connected in a loop form. The fifth and seventh MOS transistors are configured as a vertical structure, the fifth MOS transistor is laminated over the sixth MOS transistor, and the seventh MOS transistor is laminated over the eighth MOS transistor. Thus, a reduction in cell area is achieved.

At this time, an array pitch between adjacent bit lines in the first memory cell array and an array pitch between adjacent bit lines in the second memory cell array are made equal to each other to thereby make it possible to share the bit lines between the first memory cell array and the second memory cell array.

When the bit line array pitches are different from each other between the first memory cell array and the second memory cell array, a selector for selectively connecting the bit lines in the first and second memory cell arrays may preferably be interposed between the bit lines of the first memory cell array and the bit lines of the second memory cell array.

There is provided a semiconductor memory device which includes a memory cell provided at a spot where a

word line and bit lines intersect, a column selection switch for selectively connecting the bit lines to a data line, a bit line precharge circuit for precharging each of the bit lines to a predetermined level, and high voltage precharge means capable of precharging the bit line selected by the column selection switch at a voltage of a level higher than a precharge voltage outputted by the bit line precharge circuit.

According to the above means, the high voltage precharge means performs precharge at the voltage of the level higher than the precharge voltage produced by the bit line precharge circuit. This achieves a reduction in standby current and the speeding up of reading and writing.

At this time, the semiconductor memory device includes a write amplifier connected to the bit lines via the column selection switch and capable of writing data into the corresponding memory cell through the bit line selected by the column selection switch. The high voltage precharge means can be contained in the write amplifier.

The memory device can comprise including a storage section comprising an n channel type first MOS transistor and an n channel type second MOS transistor connected to each other, a p channel type third MOS transistor capable of connecting a drain electrode of the first MOS transistor and a gate electrode of the second MOS transistor to a first bit line, and a p channel type

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fourth MOS transistor capable of connecting a drain electrode of the second MOS transistor and a gate electrode of the first MOS transistor to the first bit line. The third and fourth MOS transistors are configured as a vertical structure, the third MOS transistor is laminated over the first MOS transistor, and the fourth MOS transistor is laminated over the second MOS transistor, whereby a reduction in cell area is achieved.

Also the semiconductor memory device can include a power supply circuit capable of supplying a voltage set on the condition that a difference between a source potential applied to each of the first and second MOS transistors and a potential of a select level of the word line becomes greater than or equal to a threshold voltage of each of the third and fourth MOS transistors, to a source electrode of each of the first and second MOS transistors.

Further, each of the third and fourth MOS transistors can be set so as to retain data on the high level side in the storage section in a state in which a potential opposite in polarity to a potential for turning on a channel is being applied between a gate and source thereof. When the bit lines are boosted or stepped up, the potential of the corresponding word line is relatively reduced. Hence only some of all of non-selected memory cells on the same bit line are placed in a selected state so that a large current is used up.

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However, if the data is retained in the state in which the potential opposite in polarity to the potential for turning on the channel is being applied between the gate and source as described above, then a leak current needs not increase even if the potential of each bit line rises.

The film thickness of each MOS transistor employed in a semiconductor integrated circuit is generally often limited to two types. In order to form high-withstand MOS transistors for the internal circuit within its range, MOS transistors identical in type to high-withstand MOS transistors used in an input/output circuit may preferably be used at spots where the voltage of the level higher than the precharge voltage outputted by the precharge circuit is used.

Brief Description of the Drawings

Fig. 1 is a block diagram showing a configurational example of a principal part of a mixed semiconductor memory device illustrated as one example of a semiconductor memory device according to the present invention;

Fig. 2 is a circuit diagram illustrating a configurational example of a 6T cell included in the mixed semiconductor memory device;

Fig. 3 is a circuit diagram depicting a configurational example of a 4T cell included in the mixed semiconductor memory device;

Fig. 4 is a cut cross-sectional view showing a principal part of the 4T cell;

Fig. 5 is a layout plan view illustrating a bulk-configured cell intended for comparison with the 4T cell;

Fig. 6 is an explanatory view depicting the relationship between a hold state of the 4T cell and main node voltages at that time;

Fig. 7 is an explanatory view depicting the relationship between a write state of the 4T cell and main node voltages at that time;

Fig. 8 is a waveform diagram illustrating main operations at reading and writing of the 4T cell;

Fig. 9 is a diagram for describing the relationship between various internal voltages used in a memory cell array unit;

Fig. 10 is a block diagram showing a configurational example of a semiconductor integrated circuit including a semiconductor memory device according to the present invention;

Fig. 11 is a circuit diagram illustrating a detailed configurational example of an SRAM macro included in the semiconductor integrated circuit shown in Fig. 10;

Fig. 12 is a diagram for describing the relationship between a main amplifier included in the SRAM macro and a cut cross-section of a transistor included therein;

Fig. 13 is a characteristic diagram illustrating leak currents of a transfer MOS included in the SRAM macro and drive MOSs included therein;

Fig. 14 is a diagram illustrating ON current characteristics of the n channel MOS transistors included in the SRAM macro; and

Fig. 15 is a waveform diagram showing operations of principal parts in the SRAM macro.

Detailed Description of the Preferred Embodiments

A mixed semiconductor memory device illustrated as one example of a semiconductor memory device according to the present invention is shown in Fig. 1. Although not restricted in particular, the mixed semiconductor memory device 10 shown in Fig. 1 is formed over one semiconductor substrate such as a monocrystal silicon substrate or the like by the known semiconductor integrated circuit manufacturing technology.

Although not restricted in particular, the mixed semiconductor memory device 10 includes a memory cell array unit 25, word drivers 20 and 21, a Y (column) selector 24, a main amplifier 11 and a write amplifier 12.

The memory cell array unit 25 comprises including a plurality of word lines, a plurality of bit lines respectively disposed so as to intersect them, and a plurality of memory cells respectively disposed at spots where the word lines and the bit lines intersect

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respectively. The memory cell array unit 25 is formed with a 4T cell area 13, a 4T cell area 14, a 4T cell area 15, a 6T cell area 16, a 6T cell area 17, a 6T cell area 18 and a DRAM cell area 19. A plurality of the memory cells formed by combinations of four transistors are respectively provided in the 4T cell areas 13, 14 and 15 in an array form. A plurality of the memory cells respectively formed by combinations of six transistors are respectively provided in the 6T cell areas 16, 17 and 18 in an array form. A plurality of dynamic memory cells are provided in the DRAM cell area 19 in an array form.

A power supply wiring 26 is provided between the 4T cell areas 13 and 14 and the 6T cell areas 17 and 18. A power supply wiring 27 is provided between the 4T cell area 15 and the 6T cell area 16. The memory cells (called "6T cells") formed by the combinations of the six transistors need to be supplied with a power supply VDD on the high potential side as distinct from the memory cells (called "4T cells") formed by the combinations of the four transistors. The supply of the power supply VDD on the high potential side to the 6T cells is performed via the power supply wirings 26 and 27.

Sine the 4T memory cell can be made smaller than the 6T memory cell in chip occupied area, the array pitch between the adjacent bit lines can also be narrowed correspondingly. A bit line array pitch in the 4T cell area 14 is set to 1/2 of a bit line array bit in the 6T

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cell area 18. Therefore, a sense amplifier & 1/2 selector 22 is disposed between the 4T cell area 14 and the 6T cell area 18. The bit lines in the 4T cell area 14 and the bit lines in the 6T cell area 18 are respectively connected in the form of 2 : 1. That is, one bit line in the 6T cell area 18 is connected to the two bit lines in the 4T cell area 14 via the 1/2 selector. The operation of the 1/2 selector can be controlled based on a column address signal. The sense amplifier in the sense amplifier & 1/2 selector 22 amplifies a signal read from the 4T cell area 14 to a level writable into the 6T cell area 18 and amplifies a signal read from the 6T cell area 18 to a level rewritable into the 4T cell area 14. The sense amplifier in the sense amplifier & 1/2 selector 22 is connected to the Y selector 24 on the 4T cell area 14 side, where a bit line corresponding to a column address is selected. Incidentally, contrivances such as separation of the bit lines on the 4T cell area 14 side from the sense amplifier, execution of writing into the 4T cell area 14 side by pulse driving are made after sense completion by the sense amplifier for the purpose of disturb measures taken in the 4T cell area 14.

The array pitch between the adjacent bit lines in the 4T cell area 13 is made equal to that between the adjacent bit lines in the 6T cell area 17 to thereby make common the bit lines in the 4T cell area 13 and the bit lines in the 6T cell area 17. They can be selected by the

Y selector 24 in accordance with column addresses.

The relationship between the 4T cell area 15 and the 6T cell area 16 is equal to the relationship between the 4T cell area 13 and the 6T cell area 17. That is, the array pitch between the adjacent bit lines in the 4T cell area 15 is made equal to that between the adjacent bit lines in the 6T cell area 16 to thereby make common the bit lines in the 4T cell area 15 and the bit lines in the 6T cell area 16. They can be selected by the Y selector 24 in accordance with column addresses.

The word driver 21 is shared among the 4T cell areas 13, 14 and 15 and the 6T cell areas 16, 17 and 18.

The word lines in the DRAM cell area 19 are respectively driven to a select level by the dedicated word driver 20. Each of the dynamic memory cells connected to the intersecting points of the word lines and the bit lines is formed of one transistor and a charge storage capacitor. A chip occupied area thereof is smaller than that of each of the memory cells in the 4T cell area 15 and the 6T cell area 16. Correspondingly, the array pitch between the adjacent bit lines in the DRAM cell area 19 is made smaller than the bit line array pitches in the 4T cell area 15 and the 6T cell area 16. Therefore, a sense amplifier & 1/2 selector 23 is disposed between the DRAM cell area 19 and the 6T cell area 16 in a manner similar to one disposed between the 4T cell area 14 and the 6T cell area 18, whereby the bit

lines in the DRAM cell area 19 and the 6T cell area 16 are connected in the form of 2 : 1. The operation of the 1/2 selector in the sense amplifier & 1/2 selector 23 can be controlled based on a column address signal.

A configurational example of a 6T cell 200 applied to each of the 6T cell areas 16, 17 and 18 is shown in Fig. 2.

A first inverter INV1 comprising a p channel type MOS transistor 201 and an n channel type MOS transistor 205 both connected in series, and a second inverter INV2 comprising a p channel type MOS transistor 202 and an n channel type MOS transistor 206 both connected in series are connected in a loop form to form a storage section. Source electrodes of the p channel type MOS transistors 201 and 202 are connected to a power supply VDD on the high potential side, and source electrode of the n channel type MOS transistors 205 and 206 are connected to a power supply VSS on the low potential side. Although not restricted in particular, the power supply VSS on the low potential side is equal to a ground GND line in the present semiconductor memory device. The potential thereof is set to 0 volt.

A point or spot where the p channel type MOS transistor 201 and the n channel type MOS transistor 205 are connected in series, is configured as a first node N1 of the storage section. The first node N1 is connected to a bit line BLT via an n channel type MOS transistor 203.

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A spot where the p channel type MOS transistor 202 and the n channel type MOS transistor 206 are connected in series, is configured as a node N2 of the storage section. The node N2 is connected to a bit line BLB via an n channel type MOS transistor 204. The bit lines BLT and BLB are provided as a complementary bit line pair for transmitting signals of complementary levels.

The n channel type MOS transistors 203 and 204 are operation-controlled by a potential of a word line WL. In the present example, when the word line WL is driven to a high level, the n channel type MOS transistors 203 and 204 are brought into conduction so that the first node N1 and the second node N2 of the storage section are respectively connected to the bit lines BLT and BLB, thus making it possible to write data into the storage section and read data from the storage section.

The p channel type MOS transistors 201 and 202 are configured as a vertical structure. As will be described later, the p channel type MOS transistor 201 is laminated over the n channel type MOS transistor 205, and the p channel type MOS transistor 202 is laminated over the n channel type MOS transistor 206, whereby a reduction in the area of the memory cell can be achieved.

While the 6T cell 200 shown in Fig. 2 has an advantage that it is activated at high speed in a complete static operation and low in current consumption at standby, the number of constituent elements increases

and the number of connections between the nodes also increases. Therefore, the size per cell becomes relatively large.

A configurational example of a 4T cell 300 applied to each of the 4T cell areas 13, 14 and 15 is shown in Fig. 3.

n channel type MOS transistors 305 and 306 are also referred to as drive MOSs and connected to each other to constitute a storage section. Source electrodes of the n channel type MOS transistors 305 and 306 are connected to a power supply VSS on the low potential side. A spot where a drain electrode of the n channel type MOS transistor 305 and a gate electrode of the n channel type MOS transistor 306 are connected to each other, is configured as a first node N3 of the storage section. The first node N3 is connected to a bit line BLT via a p channel type MOS transistor 301. A spot where a drain electrode of the n channel type MOS transistor 306 and a gate electrode of the n channel type MOS transistor 305 are connected to each other, is configured as a second node N4 of the storage section. The second node N4 is connected to a bit line BLB via a p channel type MOS transistor 302.

The p channel type MOS transistors 301 and 302 are also referred to as transfer MOSs and operation-controlled by a potential of a word line WL. In the present example, when the word line WL is driven to a low

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level, the p channel type MOS transistors 301 and 302 are brought into conduction so that the first node N3 and the second node N4 of the storage section are connected to their corresponding bit lines BLT and BLB, thus making it possible to write data into the storage section and read data from the storage section.

The p channel type MOS transistors 301 and 302 are configured as a vertical structure. As will be described later, the p channel type MOS transistor 301 is laminated over the n channel type MOS transistor 305, and the p channel type MOS transistor 302 is laminated over the n channel type MOS transistor 306, whereby a reduction in the area of the memory cell can be achieved.

The 4T cell 300 shown in Fig. 3 holds a high level attributable to leaks of the p channel type MOS transistors 301 and 302. Since the number of constituent elements is small and the number of nodes is also small as compared with the configuration shown in Fig. 2, the size per cell is relatively small but a trade-off relation is established between a standby current and an operating speed of the 4T cell. When a reduction in the standby current is made, for example, the operating speed is reduced correspondingly.

A layout plan of a bulk 4T cell intended for comparison with the 4T cell 300 is shown in Fig. 5. Since four transistors are constituted of bulks, the bulk 4T cell needs to provide spaces corresponding to the four

MOS transistors for their underbeds or underlying bases.
Since the p channel type MOS transistors and the n
channel type MOS transistors exist, well separation is
required. For the purpose of wiring between a p channel
region and an n channel region, all must go through an
upper layer. At this time, contact holes (LCONT and
LCONT2) for connecting diffusion layers and wiring layers
are needed.

A cross-section of a principal part of the 4T cell
300 is shown in Fig. 4. Incidentally, spots designated at
①, ② and ③ in Figs. 3 and 4 are provided to make their
corresponding definitization of the electrodes of the
main transistors.

Since the vertical structure-type p channel type
MOS transistors 301 and 302 are formed in the form of
being laminated over the n channel type MOS transistors
305 and 306, spaces corresponding to the two MOS
transistors are enough for underbeds or underlying bases.
Since the p channel type MOS transistors 301 and 302 are
of SOI, well separation is not necessary. Since they
themselves share contacts because of the vertical
structure, there is no need to provide the contact holes
essential to the bulk constitution.

Since the p channel type MOS transistors are used
for transfer MOSs (301 and 302) in the 4T cell 300, a
high level in the cell is raised to the potential of each
bit line upon data writing. However, a low level enables

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writing only up to VSS – Vth. Here, Vth is defined as the threshold voltage of each of the transfer MOSs (301 and 302). Therefore, "0" write compensation is performed in the following manner.

Fig. 6 shows the relationship between a hold state of the 4T cell 300 and main node voltages at that time.

A leak of the p channel type MOS transistor 301 or 302 compensates for a voltage drop developed by a leak at the turning off of the n channel type MOS transistor at the node N3 or N4 brought to a high level (logical value "1"). Therefore, the p channel type MOS transistor 301 or 302 is controlled to a very shallow on state (Vgs = α). Thus, the same current as described above flows even into the node N3 or N4 brought to a low level (logical value "0"). At this time, however, it flows into the low-potential power supply VSS side via the n channel MOS transistor 305 or 306 placed in an on state. A node Vssm potential (+β) in the hold state is generated using the above current and used as a "0" write compensation potential.

Fig. 7 shows the relationship between a write state of the 4T cell 300 and main node voltages at that time.

Upon writing, the word line WL is brought to a low level (= VSS), so that the p channel type MOS transistors 301 and 302 are brought into conduction. Since the bit line BLT is high in level (= VDD), they are operated in a common-source configuration with the level of the power

supply VDD level on the high potential side as the reference. Since, however, the potential ratio of the above transistor to the n channel type MOS transistor 305 is taken, the node N3 simply rises to about 1/3 when kept intact. Since the driving of the n channel type MOS transistor 305 becomes weak as the potential of the node N4 side decreases, it gradually rises and finally reaches the power supply VDD level on the high potential side. Since the node N4 side is initially brought to the power supply VDD level in reverse, the common-source configuration is taken. Further, the potential of the node N4 side drops rapidly because of no load MOS transistor. However, as the potential of the node N4 side gradually approaches the Vssm level, a gate-to-source voltage Vgs is reduced, so a source-follower operation is taken. Finally, Vgs = Vssm - Vss is achieved. Here, the level of Vssm is determined so that Vgs reaches greater than or equal to the threshold voltage of each of the p channel type MOS transistors 301 and 302. Consequently, "0" write compensation is carried out. Incidentally, even if a slight voltage remains at each node in some cases, any of the nodes becomes the Vssm level by the leak of the p channel type MOS transistor 301 or 302.

Fig. 8 shows main operational waveforms at reading and writing of the 4T cell 300.

In the case of a selected cell, the word line W1 is driven to a low level. During a read period, the word

line WL is reduced to a power supply VSS level on the low potential side so that signals at the nodes N3 and N4 are read into the bit lines BLT/BLB. During a write period, the word line WL is reduced to the power supply VSS level, so that write data is transferred to each of the nodes N3 and N4. At this time, the low level of each bit line is made higher by the threshold voltage of each transfer MOS than the select level (power supply VSS level on the low potential side) of the word line WL, whereby "0" write compensation is performed.

Various internal voltages used in the memory cell array unit 25 are shown in Fig. 9.

A high level of each bit line is set to 1.7V, and a low level of each bit line is set to 0V (= VSS). A high level (non-select level) of a word line is set to 1.2V, and a low level (select level) of the word line is set to 0V (= VSS). A Vssm level (cell VSS) of the 4T cell 300 is set to 0.3V in consideration of "0" write compensation. This is one determined in such a manner that Vgs becomes greater than or equal to the threshold voltage of each of the p channel type MOS transistors 301 and 302 when Vgs = Vssm - Vss. Such various voltages are obtained by stepping down a voltage given from outside in the following manner.

That is, a power supply voltage 1.5V (VDD) supplied from outside is stepped down by a step-down circuit 91 to thereby generate an internal 1.2V voltage to be supplied

to each of peripheral circuits. The power supply voltage 1.5V (VDD) supplied from outside is stepped down by a step-down circuit 92 to thereby generate 1.2V corresponding to the high level of the word line WL. Since the generated 1.2V stabilizes a retention or hold characteristic, trimming and temperature compensation have been made. This voltage is stabilized by a parasitic capacitor C1 at a non-selected word line. Cell VDD = 0.3V is stabilized by a constant voltage circuit 93 and a parasitic capacitor C2 in a memory cell array. The constant voltage circuit 93 is connected to the source electrodes of the n channel MOS transistors 305 and 306 in the 4T cell 300 and the power supply VSS on the low potential side, and serves as variable impedance means with respect to a cell current. Although not restricted in particular, the constant voltage circuit 93 comprises including an n channel type MOS transistor 933 connected to the source electrodes of the n channel MOS transistors 305 and 306 in the 4T cell 300 and the power supply VSS on the low potential side, a reference voltage generator 931 for generating a reference voltage Vref, based on the power supply voltage 1.5V (VDD) supplied from outside, and an error amplifier 932 for determining the difference between the reference voltage Vref generated by the reference voltage generator 931 and the cell VSS and controlling the on resistance of the n channel type MOS transistor 933, based on the difference. The reference

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voltage generator 931 stabilizes the reference voltage Vref according to trimming and temperature compensation. That is, the reference voltage generator 931 is provided with a stable reference voltage source such as a bandgap reference, and a fuse circuit capable of trimming upon testing, and a pseudo or dummy trimming circuit. Variations between lots of p channel type MOS transistors are corrected by the trimming function to thereby make it possible to achieve an improvement in yield. Owing to the dummy trimming function, a voltage level is changed according to a test command without causing a fuse to blow, thereby attempting to facilitate a write margin test.

According to the above example, the following operation and effects can be obtained.

(1) In general, the density of a memory cell is reduced in order of the DRAM cell area, 4T cell area and 6T cell area. A random access speed is lowered in order of the 6T cell area, 4T cell area and DRAM cell area. Thus, preferably, data large in its amount and in which an access speed is not so emphasized is stored in the DRAM area 19, and data high in use frequency and in need of high-speed access is stored in each of the 6T cell areas 16, 17, 18 and 4T cell areas 13, 14 and 15. The cell areas are used properly according to the requests of the access speed, the use frequency, etc. in this way to thereby obtain the maximum performance. Since the bit

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line is brought into conduction between the different
cell areas, the copy of each stored data can be performed
at high speed via the bit line. When, for example, the
data stored in the 6T cell areas 16, 17 and 18 are
transferred to the 4T cell areas 13, 14 and 15
respectively, high-speed data transfer is enabled using
the bit lines brought into conduction.

(2) Since the cell VDD = 0.3V is formed to perform
the "0" write compensation, writing exceeding the limit
of VSS - Vth is enabled upon writing of the low level.
Also the cell VDD = 0.3V is stabilized by the constant
voltage circuit 93, and the parasitic capacitor C2 in the
memory cell array. The constant voltage circuit 93 is
connected to the source electrodes of the n channel type
MOS transistors 305 and 306 in the 4T cell 300, and the
power supply VSS on the low potential side, and serves as
the variable impedance means with respect to the cell
current. The constant voltage circuit 93 comprises
including the n channel type MOS transistor 933 connected
to the source electrodes of the n channel MOS transistors
305 and 306 in the 4T cell 300 and the power supply VSS
on the low potential side, the reference voltage
generator 931 for generating the reference voltage Vref,
based on the power supply voltage 1.5V VDD supplied from
outside, and the error amplifier 932 for determining the
difference between the reference voltage Vref generated
by the reference voltage generator 931 and the cell VSS

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and controlling the on resistance of the n channel type MOS transistor 933, based on the difference, whereby the stabilization of the cell VDD = 0.3V is achieved.

(3) Since the p channel MOS transistors 301 and 302 of vertical structure are applied to the transfer MOSs, and the p channel type MOS transistors 301 and 302 of vertical structure are formed in the form of being heaped up over the n channel type MOS transistors 305 and 306, the spaces corresponding to the two MOS transistors are enough for the underlying bases. Since the p channel type MOS transistors 301 and 302 are of SOI, the well separation is not necessary. Since they themselves share the contacts because of the vertical structure, there is no need to provide the contact holes essential to the bulk constitution. From this point of view, the scaling down of the memory cell can be achieved.

A configurational example of a semiconductor integrated circuit including a semiconductor memory device according to the present invention is shown in Fig. 10.

Although not restricted in particular, the semiconductor integrated circuit 100 shown in Fig. 10 includes an input circuit 101, a level shifter 102, an internal logic 103, a level shifter 104, an output circuit 105, a step-down power supply circuit 106 and an SRAM macro 107 and is formed over one semiconductor substrate such as a monocrystal silicon substrate by the

known semiconductor integrated circuit manufacturing technology. The input circuit 101 has the function of fetching or taking in a signal inputted via an input terminal. The level shifter 101 has the function of shifting a signal of a power supply VDD system (high voltage) on the high potential side, which is inputted via the input circuit 101, to a Vperi system (low voltage). The internal logic 103 is of a Vperi system and includes a central processing unit for effecting a predetermined logical operating process on the input signal, and peripheral circuits thereof. Upon the logical operation of the internal logic 103, the SRAM macro 107 is accessed and information stored therein is used as needed. The level shifter 104 has the function of shifting a signal (Vperi system) outputted from the internal logic 103 to the power supply VDD system on the high potential side. The output circuit 105 has the function of outputting a signal outputted from the level shifter 104 from an output terminal.

The step-down power supply circuit 106 steps down the supplied power supply VDD on the high potential side to thereby generate a voltage Vperi lower than a VDD level. The generated voltage Vperi is supplied to the level shifter 102, the internal logic 103, the level shifter 104 and the SRAM macro 107.

Although not restricted in particular, the SRAM macro 107 includes a Y (column) decoder 108, a main

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amplifier and write amplifier 109, a column selection circuit 110, an SRAM mat 111, a VSSM generator 112, a VWL generator 113 and a word line driver 114.

A configurational example of a principal part of the SRAM macro 107 is shown in Fig. 11.

The SRAM mat 111 includes a plurality of word lines, a plurality of bit lines provided so as to intersect the word lines, and a plurality of 4T cells respectively provided at spots where the word lines and the bit lines intersect respectively. Ones each having the same configuration as one shown in Fig. 3 are basically applied to the 4T cells. That is, n channel type MOS transistors 305 and 306 are connected to constitute a storage section. Source electrodes of the n channel type MOS transistors 305 and 306 are connected to a power supply Vssm on the low potential side. A spot where a drain electrode of the n channel type MOS transistor 305 and a gate electrode of the n channel type MOS transistor 306 are connected to each other, is configured as a first node N3 of the storage section. The first node N3 is connected to a bit line BLT via a p channel type MOS transistor 301. A spot where a drain electrode of the n channel type MOS transistor 306 and a gate electrode of the n channel type MOS transistor 305 are connected to each other, is configured as a second node N4 of the storage section. The second node N4 is connected to a bit line BLB via a p channel type MOS transistor 302.

The p channel type MOS transistors 301 and 302 are operation-controlled by a potential of a word line WL. In the present example, when the word line WL is driven to a low level, the p channel type MOS transistors 301 and 302 are brought into conduction so that the first node N3 and the second node N4 of the storage section are respectively connected to the bit lines BLT and BLB, thus making it possible to write data into the storage section and read data from the storage section.

The p channel type MOS transistors 301 and 302 are configured as such a vertical structure as shown in Fig. 4. The p channel type MOS transistor 301 is laminated over the n channel type MOS transistor 305, and the p channel type MOS transistor 302 is laminated over the n channel type MOS transistor 306, whereby a reduction in the area of the memory cell can be achieved.

The VSSM generator 112 is configured in a manner similar to the constant voltage circuit 93 shown in Fig. 9 by way of example and performs "0" write compensation.

The plurality of word lines WL are selectively driven by a word line driver (WLD) 120. The word line driver 120 decodes an input X (row) address signal and drives one corresponding to the X address from the plurality of word lines WL to a select level, based on the result of decoding. In the present example, since the p channel type MOS transistors 301 and 302 are applied as transfer MOSs in the 4T cell 300, the select level of the

word line WL is brought to a low level, which is equal to a power supply VSS level on the low potential side.

A VWL generator 121 controls a drive potential level of each word line, based on the ratio between leak currents of a p channel MOS transistor and an n channel type MOS transistor.

The complementary bit lines BLT and BLB are selectively connected to the main amplifier and write amplifier 109 via the column selection circuit 110. The main amplifier and write amplifier 109 includes a main amplifier MA for amplifying a signal transmitted through the column selection circuit 110, and a write amplifier MA for supplying write data to the bit lines BLT and BLB through the column selection circuit 110.

The column selection circuit 110 is configured as follows:

A p channel type MOS transistor 135 and an n channel type MOS transistor 136 are connected in parallel to form a column switch. The bit line BLT is connected to the main amplifier MA and the write amplifier WA through the column switch. A p channel type MOS transistor 137 and an n channel type MOS transistor 138 are connected in parallel to form a column switch. The bit line BLB is connected to the main amplifier MA and the write amplifier WA through the column switch. There is further provided a precharge circuit for precharging each of the bit lines BLT and BLB to a predetermined voltage level.

The precharge circuit comprises a p channel type MOS transistor 132 connected to the bit line BLT and a p channel type MOS transistor 133 connected to the bit line BLB, both of which are connected in series. A node where the p channel type MOS transistors 132 and 133 are connected in series, is supplied with a precharge voltage VbHold of a predetermined level. A column select signal Ys is transferred to gate electrodes of the p channel type MOS transistors 132 and 133. When the column select signal Ys is asserted low in level, the p channel type MOS transistors 132 and 133 are brought into conduction so that the bit lines BLT and BLB are precharged by the precharge voltage VbHold. A p channel type MOS transistor 131 for equalize is provided so as to short-circuit the bit lines BLT and BLB. When the column select signal Ys is asserted low in level so that the bit lines BLT and BLB are supplied with the precharge voltage VbHold, the p channel type MOS transistor 131 for equalize is brought into conduction so that the bit lines BLT and BLB are made equal to each other in precharge level.

The main amplifier MA comprises p channel type MOS transistors 139 and 140, and n channel type MOS transistors 141, 142, 143, 144 and 145 all of which are connected to one another. A series-connected circuit of the MOS transistors 139, 141 and 143 and a series-connected circuit of the MOS transistors 140, 142 and 144 are connected in a loop form to form a latch circuit.

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Source electrodes of the p channel type MOS transistors 139 and 140 are supplied with a voltage Vperi. Source electrodes of the n channel type MOS transistors 143 and 144 are connected to the power supply VSS on the low potential side through the n channel type MOS transistor 145. A main amplifier enable signal MAE is transferred to a gate electrode of the n channel type MOS transistor 145. When the main amplifier enable signal MAE is asserted high in level so that the n channel type MOS transistor 145 is brought into conduction, the main amplifier MA is brought to an enable or operable state.

The main amplifier WA comprises p channel type MOS transistors 146, 148 and 150, and p channel type MOS transistors 147 and 149 all of which are connected to one another. The p channel type MOS transistor 146 and the n channel type MOS transistor 147 are connected in series. A spot where they are connected in series, is configured as a node IT, which is connected to the bit line BLT via the MOS transistors 135 and 136 of the column selection circuit 110. The p channel type MOS transistor 148 and the n channel type MOS transistor 149 are connected in series. A spot where they are connected in series, is configured as a node IB, which is connected to the bit line BLB via the MOS transistors 137 and 138 of the column selection circuit 110. A gate electrode of the p channel MOS transistor 146 is supplied with a step-up control ITUB for the node IT. When the step-up control

signal ITUB is asserted low in level, the p channel type MOS transistor 146 is brought into conduction so that a high voltage based on a power supply VDD on the high potential side is supplied to the node IT. A gate electrode of the p channel MOS transistor 148 is supplied with a step-up control signal IBUB for the node IB. When the step-up control signal IBUB is asserted low in level, the p channel type MOS transistor 148 is brought into conduction so that a high voltage based on the power supply VDD on the high potential side is supplied to the node IB.

Source electrodes of the n channel type MOS transistors 147 and 149 are connected to the power supply VDSS on the low potential side. Gate electrodes of the n channel type MOS transistors 147 and 149 are supplied with write data ITD and IBD. The operations of the n channel type MOS transistors 147 and 149 are controlled in accordance with the write data ITD and IBD to enable data writing.

Further, a p channel type MOS transistor 150 is provided so as to short-circuit the nodes IT and IB. The nodes IT and IB are equalized in accordance with an equalize control signal IEQB transferred to a gate electrode of the p channel type MOS transistor 150.

Here, a cell read current and a leak current are proportional to each other in the 4T cell 300. This means that a high speed operation and a low leak are

incompatible. That is, when the threshold voltage is
lowered for the high speed operation to ensure a
sufficient gate-to-source voltage Vgs, a large standby
current flows. When the threshold voltage is made high to
lower a drain-to-source voltage Vds in reverse, a small
read current flows so that a low speed operation is
enabled.

Although the cell VSS is raised in a standby mode
to achieve a reduction in leak current, there is a need
to set each mode, and frequent standby cannot be
performed.

Thus, the SRAM macro 107 shown in Fig. 10 makes use
of MOS transistors (thick film elements) high in
threshold voltage. Then Vbl is lowered during a period
other than reading to make a low leak state, and a bit
line selected by a column selection system (Ys) is
boosted or stepped up upon reading, thereby enabling a
reduction in current consumption and high-speed reading
of data.

That is, thick film elements (high-withstand MOS
transistors) are applied to all the MOS transistors
constituting the 4T cell 300, all the MOS transistors
constituting the column selection circuit 110, all the
MOS transistors constituting the write amplifier WA, and
the MOS transistors 141 and 142 in the main amplifier MA,
whereby their threshold voltages are set high and besides
a bit line precharge voltage VblHold is set low.

Fig. 12 typically shows a cross-sectional structure of a principal part of the main amplifier MA.

The main amplifier MA is configured as a portion where the VDD system is switched to the Vperi system. Only the n channel type MOS transistors 141 and 142 are configured as thick film elements, and other MOS transistors are configured as thin film elements. The thickness of an oxide film of the gate of each thick film element is made thicker than that of a gate oxide film of other MOS transistor, e.g., the thin film MOS transistor 143.

Using such thick film elements enables a reduction in standby current. Since, however, only a small read current is obtained upon reading of data from the 4T cell 300 if kept intact, time is taken to read the data. Therefore, in the present example, the high voltage (power supply VDD on the high potential side) is supplied to the bit lines BLT BLB each selected in accordance with the column select signal Ys through the nodes IT and IB to thereby raise the precharge levels of the bit lines. Consequently, the data can be read at high speed from the 4T cell 300. Even upon writing of data into the 4T cell 300, the high voltage (power supply VDD on the high potential side) is supplied to the bit lines BLT and BLB via the nodes IT and IB in the same manner as described above, whereby the precharge levels of the bit lines are raised to achieve the speeding up of writing.

In the present example, as described above, the high voltage (power supply VDD on the high potential side) is supplied via the nodes IT and IB to raise the precharge levels of the bit lines, whereby the reading of the data from the 4T cell 300 at high speed is enabled. Thus, the high-withstand MOS transistors are used at spots where the voltage higher than the precharge voltage is supplied. In the configurational example shown in Fig. 11 by way of example, all the MOS transistors constituting the 4T cell 300, all the MOS transistors constituting the column selection circuit 110, all the MOS transistors constituting the write amplifier WA, and the MOS transistors 141 and 142 of the main amplifier MA are configured as high-withstand MOS transistors. At this time, ones identical in type to the high-withstand MOS transistors used in the input circuit 101 and output circuit 105 shown in Fig. 10 are used for high-withstand MOS transistors used in the internal circuit. This is because the film thickness of each MOS transistor employed in a semiconductor integrated circuit is generally often limited to two types, and the high-withstand MOS transistors of the internal circuit can be formed within its range.

Leak current characteristics of transfer MOSs (p channel type MOS transistors 301 and 302) and drive MOSs (n channel type MOS transistors 305 and 306) are shown in Fig. 13. The horizontal axis indicates a gate-to-source

voltage of each MOS transistor, and the vertical axis
indicates a drain-source current of each MOS transistor.
Characteristic curves indicated by solid lines correspond
to the case where the potential of each bit line BL =
1.5V, whereas characteristic curves indicated by broken
lines correspond to the case where the potential of each
bit line BL = 2.0V. ON current characteristics are
illustrated in Fig. 14.

A potential opposite in polarity to a potential for
turning on a channel is applied between the gate and
source to increase a leak current. This is known as the
GIDL (Gate Induced Drain Leakage) characteristic. In the
present example, such a GIDL characteristic is used to
retain or hold data. Incidentally, the GIDL
characteristic of the MOS transistor has been described
in, for example, "Ja-Hao, Chen, Shyh-Chyi Wong, and
Yeong-Her Wang "An Analytic Three-Terminal Band-to-Band
Tunneling Model on GIDL in MOSFET" IEEE TRANSACTIONS ON
ELECTRON, VOL. 48, 7, JULY 2001".

Referring to Fig. 13, since the potential of the
bit line BL = 2.0V upon reading, a gate-to-source voltage
Vgs of each transfer MOS results in -0.1V. Thus, the
transfer MOS is held ON very weakly by the GIDL
characteristic and hence a leak current increases
slighter than usual. With the use of this mode, restoring
of each non-selected cell can be speeded up.

The retention of data is performed in a GIDL region

of a p channel type MOS transistor. That is, each of the
transistors is set so as to hold or retain data on the
high level side in the storage section in a state in
which the potential opposite in polarity to the potential
for turning on the channel is being applied between the
gate and source. This results from the following reasons.

That is, when the bit lines are boosted or stepped
up, the potential of the corresponding word line is
relatively reduced. Only some of all the non-selected
memory cells on the same bit line are placed in a
selected state so that a large current is used up.
However, if the high level of data is retained using the
GIDL region of the p channel type MOS transistor, then
the leak current needs not increase even if the potential
of each bit line rises.

Thus, in the present example, the potential BL of
the bit line is +0.4V (1.5V + 0.4V = 1.9V) and the gate-
to-source voltage Vgs is given as a reverse bias of 0.4V
at idle. Therefore, the word line WL retains a high level
by use of the GIDL region. An off leak current of each
drive MOS (corresponding to each of n channel type MOS
transistors 305 and 306) results in 10^{-13}[A] if BL = 1.5V.
This current results in 1/50 as compared with 5×10^{-12} at
BL = 2.0V of a read voltage.

Since the standby current is set to 50 to 100 times
the leak current of the drive MOS, the standby current
can be brought to $10^{-13} \times 100 = 10^{-11}$ when BL = 1.5V, and

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1/20 of 2 x 10^{-12} x 100 = 2 x 10^{-10} when BL = 2.0V. When BL = 2.0V is set, 4.0mA is obtained with respect to 1.1mA at BL = 1.5V upon reading, so that an increase (speeding up) of 3.6 times is enabled.

Operational waveforms of principal parts of the SRAM macro 107 shown in Fig. 11 are illustrated in Fig. 15. Hold periods, read periods and write periods are shown in the present example.

During the hold period, the bit lines are precharged by a low bit line precharge voltage VblHold to thereby reduce a cell leak current.

During the read period, the power supply VDD on the high potential side is applied to the main amplifier MA and the write amplifier WA. Therefore, the potentials of the bit lines BLT and BLB selected by the column selection circuit 110 rise and correspondingly the driving force of the memory cell increases. After the completion of reading, the bit lines BLT and BLB are respectively brought to a high potential level so that cell restoring is performed.

When the bit lines BLT and BLB are respectively brought to a non-selected state during a hold period set immediately after the read period, the bit lines BLB/BLT are slowly restored to the original voltage level of VblHold.

Next, during a write period, the power supply VDD on the high potential side is applied to the main

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amplifier MA and the write amplifier WA in a manner similar to the read period. Therefore, the potentials of the bit lines BLT and BLB selected by the column selection circuit 110 rise and correspondingly the driving force of the memory cell increases. After the completion of reading, the potentials of the bit lines BLT and BLB are made equal to the high potential, so that cell restoring is effected.

According to the above example, the following operation and effects can be obtained.

That is, the thick film elements are applied to all the MOS transistors constituting the 4T cell 300, all the MOS transistors constituting the column selection circuit 110, all the MOS transistors constituting the write amplifier WA, and the MOS transistors 141 and 142 of the main amplifier MA, whereby their threshold voltages are made high and besides the bit line precharge voltage VblHold is set low. It is thus possible to achieve a reduction in standby current. Upon reading, the high voltage (power supply VDD on the high potential side) is supplied to the bit lines BLT and BLB selected in accordance with the column select signal Ys via the nodes IT and IB to thereby raise the precharge levels of the bit lines, thus making it possible to read the data from the 4T cell 300 at high speed.

Even upon writing of the data into the 4T cell 300, the high voltage (power supply VDD on the high potential

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side) is similarly supplied to the bit lines BLT and BLB via the nodes IT and IB to thereby raise the precharge levels of the bit lines, thus making it possible to achieve the speeding up of the data writing.

While the invention developed above by the present inventors has been described specifically by the illustrated embodiments, the present invention is not limited to the embodiments. It is needless to say that various changes can be made thereto within the scope not departing from the substance thereof.

For instance, an FRAM (Ferroelectric RAM) area is provided in place of the DRAM cell area 19 shown in Fig. 1. Nonvolatile memory cells each having a ferroelectric film used in a capacitor for data retention may be laid out in the FRAM area.

The main amplifier MA, the write amplifier WA, the column selection circuit 110, etc. shown in Fig. 11 can be applied to the mixed semiconductor memory device shown in Fig. 1.

While the above description has principally been made of the case in which the invention made by the present inventors is applied to the semiconductor integrated circuit including the SRAM macro, which belongs to the field of application reaching the background of the invention, the present invention is not limited to it but can be widely applied to various semiconductor integrated circuits.

The present invention can be applied on the condition that at least the bit lines are included.

Advantageous effects obtained by a representative one of the inventions disclosed in the present application will be described in brief as follows:

When a memory cell comprises including first, second, third and fourth transistors, the third and fourth transistors are configured as a vertical structure, the third transistor is laminated over the first transistor, and the fourth transistor is laminated over the second transistor, whereby a reduction in cell area can be achieved. A voltage set on the condition that the difference between a source potential applied to each of the first and second transistors and a select level of a word line reaches greater than or equal to a threshold voltage of each of the third and fourth transistors, is supplied to each of source electrodes of the first and second transistors thereby to provide "0" write compensation, whereby the appropriateness of writing of a logical value "0" is achieved. High voltage precharge means performs precharge at a voltage higher than a precharge voltage from the bit line precharge circuit to thereby make it possible to achieve a reduction in standby current and the speeding up of reading and writing.